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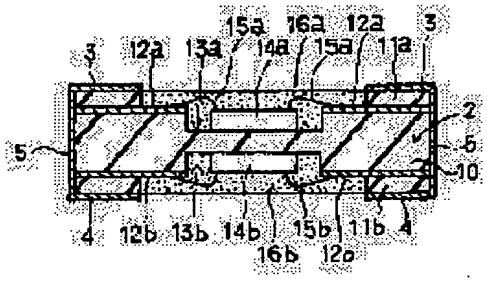
(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To realize good handling property and increase the memory capacity by attaching a semiconductor element constituting a memory into recesses on front and back sides of a wiring board and covering the semiconductor element with an insulating resin.

SOLUTION: A semiconductor device 1 has a rectangular wiring board 2, and an upper side electrode 3 and a lower side electrode 4 provided on front and back sides of the wiring board 2. The upper side electrode 3 and the lower side electrode 4 are electrically connected with each other via a lateral side electrode 5. Thus, the upper side electrode 3 and the lower side electrode 4 are vertically overlapped in a perspective view, and form electrodes of the same function. Also, semiconductor elements 14a, 14b made of memory elements are fixed on recessed front and back surfaces of the wiring board 2, respectively, and the upper side electrode 3, the lower side electrode 4 and the lateral side electrode 5 as lead-out terminals of the semiconductor elements 14a, 14b are commonly used by these semiconductor elements. Therefore, the memory capacity is increased. Since the semiconductor element is embedded in the recess of the rigid wiring board 2 and covered with resin, good handling property of the semiconductor device 1 is realized.



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CLAIMS

[Claim(s)]
[Claim 1] The connecting means which connects electrically the external electrode which is prepared in the wiring substrate of the multilayer structure which prepared the hollow which became depressed at least one step in the center of a front rear face, the semiconductor device fixed to the hollow on the rear face of front of said wiring substrate, respectively, and the front rear face of said wiring substrate, and is connected with predetermined internal wiring, and the electrode of said semiconductor device, said internal wiring or an external electrode, and the semiconductor device which are characterized by to have the closure object of wrap insulation for said semiconductor device.
[Claim 2] The electrode which said semiconductor device consists of a memory device, and the top-face lateral electrode and inferior-surface-of-tongue lateral electrode of said wiring substrate lap up and down in fluoroscopy, and laps mutually is a semiconductor device according to claim 1 characterized by being the electrode of the same function.
[Claim 3] Said semiconductor device is a semiconductor device according to claim 2 characterized by being constituted so that it may become the structure which can be piled up one by one and the top-face lateral electrode of a lower semiconductor device and the inferior-surface-of-tongue lateral electrode of a upside semiconductor device may be electrically connected by piling up.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a semiconductor device, especially an LCC (Leadless-chip carrier) mold semiconductor device.
[0002]
[Description of the Prior Art] The semiconductor device is built into the circuit board by multistage in order to attain large capacity-ization of the memory included in electronic equipment. For example, the example by which the multistage pile of the semiconductor device of TCP structure is carried out to issue and P181 on Nikkei Business Publications issue "VLSI packaging technical (below)" May 15, 1993 is indicated. Moreover, the example which the semiconductor chip (SUTATIKU RAM) which attached the lead to the front rear face of the module substrate of a dual in-line form has put on multistage,

respectively is shown in JP,64-1269,A.
[0003]
[Problem(s) to be Solved by the Invention] In order to attain large capacity-ization of memory, the semiconductor device is mounted in module substrates, such as the circuit board, in piles multistage. However, the semiconductor device of TCP structure or the structure which attached the lead to the semiconductor chip is not strong, and is dealt with, and its sex is bad.
[0004] The purpose of this invention has good handling nature, and it is to offer the semiconductor device which can attain enlargement of memory space.
[0005] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.
[0006]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0007] (1) It has the closure object (resin) of wrap insulation for the connecting means which connects electrically the external electrode which is prepared in the wiring substrate of the multilayer structure which prepared the hollow which became depressed at least one step in the center of a front rear face, the semiconductor device fixed to the hollow on the rear face of front of said wiring substrate, respectively, and the front rear face of said wiring substrate, and is connected with predetermined internal wiring, and the electrode of said semiconductor device, said internal wiring or an external electrode, and said semiconductor device. Said semiconductor device consists of a memory device, and the electrode which the top-face lateral electrode and inferior-surface-of-tongue lateral electrode of said wiring substrate lap up and down in fluoroscopy, and laps mutually is the electrode of the same function. Said semiconductor device is constituted so that it may become the structure which can be piled up one by one and the top-face lateral electrode of a lower semiconductor device and the inferior-surface-of-tongue lateral electrode of a upside semiconductor device may be electrically connected by piling up.
[0008] According to the means of the above (1), since it has structure which attached the semiconductor device which constitutes memory, respectively in the hollow on the rear face of front of the wiring substrate object which made the wiring substrate of (a) plurality rival, and covered the semiconductor device by insulating resin, memory space can offer a strong large semiconductor device.
[0009] (b) Since it is constituted so that the electrode with which a semiconductor device serves as structure which can be piled up one by one, and a lower semiconductor device and a upside semiconductor device correspond by piling up may be connected, superposition mounting can attain large capacity-ization of memory.
[0010]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing. In addition, in the complete diagram for explaining the gestalt of implementation of invention, what has the same function attaches the same sign, and explanation of the repeat is omitted.
[0011] The sectional view in which drawing 1 shows the semiconductor device of 1 operation gestalt of this invention, the top view of the semiconductor device in the condition that drawing 2 cut and lacked a part of this operation gestalt, and drawing 3 are the top views of the wiring substrate in which the wirebonding condition in manufacture of the semiconductor device of this operation gestalt is shown.
[0012] The example which applied this invention to the LCC mold semiconductor device which constitutes memory from this operation gestalt is explained. In appearance, the semiconductor device 1 of this operation gestalt has the top-face lateral electrode 3 and the inferior-surface-of-tongue lateral electrode 4 which were prepared in the front rear face of the rectangle tabular wiring substrate 2 and this wiring substrate 2, as shown in drawing 1 and drawing 2 . Moreover, said top-face lateral electrode 3 and the inferior-surface-of-tongue lateral electrode 4 are electrically connected through the side-face lateral electrode 5. Therefore, in the semiconductor device 1 of this operation gestalt, the electrode

which the top-face lateral electrode 3 and the inferior-surface-of-tongue lateral electrode 4 lap in the upper and lower sides in fluoroscopy, and laps mutually is the electrode of the same function.
[0013] Said wiring substrate 2 consists of a glass epoxy group plate, and consists of an insulating 1st glass epoxy plate 10 and frame-like 2nd glass epoxy plates 11a and 11b stuck on the front rear face of said 1st glass epoxy plate 10. Therefore, the center of a front rear face of the wiring substrate 2 serves as structure which became depressed one step.
[0014] As shown in drawing 1 thru/or drawing 3 , the wiring (internal wiring) 12a and 12b of a predetermined pattern is formed in the front rear face of said 1st glass epoxy plate 10. The outer edge part which extends on the edge of the 1st glass epoxy plate 10 of the internal wiring 12a and 12b is seen in fluoroscopy, and laps with said top-face lateral electrode 3 and the inferior-surface-of-tongue lateral electrode 4. And the outer edge part of the internal wiring 12a and 12b is electrically connected to the side-face lateral electrode 5 electrically connected with said top-face lateral electrode 3 and inferior-surface-of-tongue lateral electrode 4. Moreover, the internal wiring 12a and 12b serves as a pattern which sees in fluoroscopy and laps mutually.
[0015] Moreover, the component fixed hollows 13a and 13b for fixing a semiconductor device by seat GURI are formed in the center of said 1st glass epoxy plate 10. Thereby, the center of a front rear face of the wiring substrate 2 has two-step hollow structure.
[0016] The semiconductor devices 14a and 14b which constitute a memory device through the adhesives which are not illustrated, respectively are being fixed to said component fixed hollows 13a and 13b. A part for the electrode which said semiconductor devices 14a and 14b do not illustrate, and the toe of the internal wiring 12a and 12b is electrically connected with the conductive wires 15a and 15b.
[0017] Moreover, into the part by which the front rear face of said wiring substrate 2 became depressed, insulating resin (closure object) 16a and 16b is embedded, and semiconductor devices 14a and 14b and Wires 15a and 15b are closed into it. The front face of Resin 16a and 16b is the front face on the rear face of front of the wiring substrate 2, the flat surface of abbreviation identitas, and the flat surface that becomes. Consequently, the closure of the two semiconductor devices 14a and 14b will be carried out with the package which consists of a wiring substrate 2 and resin 16a and 16b.
[0018] The semiconductor device of this operation gestalt serves as a thin shape and small structure. For example, a semiconductor device 1 serves as die length of 16.1mm, width of face of 9.6mm, and height of about 1.2-1.5mm.
[0019] Since the semiconductor devices 14a and 14b which consist of a memory device, respectively are fixed to the front rear face at which said wiring substrate 2 became depressed and the semiconductor device 1 of this operation gestalt becomes common [the external cash-drawer terminal (the top-face lateral electrode 3, the inferior-surface-of-tongue lateral electrode 4 side-face lateral electrode 5) of each semiconductor devices 14a and 14b], memory space will become high. That is, memory space will have twice as many memory space as the semiconductor device which contained the single semiconductor device.
[0020] Since the semiconductor device 1 of this operation gestalt is built in in the hollow of the strong wiring substrate 2 and is covered by Resin 16a and 16b, it serves as strong structure and becomes good [handling nature].
[0021] The semiconductor device 1 of this operation gestalt prepares a seat GURI part in the 1st glass epoxy plate 10 of the wiring substrate 2, and since it serves as structure which fixes semiconductor devices 14a and 14b to the seat GURI part, height serves as thickness of the wiring substrate 2, and it serves as thin structure.
[0022] Although use with an item is also possible, since the semiconductor device 1 of such this operation gestalt serves as an electrode of the same function, it can also use for a multilayer two or more electrodes with which the top-face lateral electrode 3 and the inferior-surface-of-tongue lateral electrode 4 lap in the upper and lower sides in fluoroscopy, and lap mutually in piles.
[0023] That is, drawing 4 is the laminating mold semiconductor device 21 which connected two semiconductor devices 1 in piles through solder 20 by the electrode section. This laminating mold

semiconductor device 21 can increase memory space by 4 times as compared with the semiconductor device incorporating a single semiconductor device.
[0024] Said laminating mold semiconductor device 21 is SIMM (Single in-line memory module), as shown in drawing 5 . Two or more mounting is carried out together with the front rear face of a substrate 22, i.e., a memory module substrate. When the single laminating mold semiconductor device 21 is mounted in the memory module substrate 22 from the semiconductor device 1 of this operation gestalt serving as die length of 16.1mm, width of face of 9.6mm, and height of about 1.2-1.5mm, and having height of the one half of the usual SOJ mold semiconductor device, even if the mounting volume is the same, memory space increases also 4 times. Thereby, the memory space of SIMM can be increased by leaps and bounds. Since the laminating mold semiconductor device 21 also has strong structure, handling nature is good and becomes easy [the inclusion to the memory module substrate 22].
[0025] Drawing 6 is the sectional view showing the condition of having mounted the semiconductor device 1 of this operation gestalt between substrate 25a of the pair of a memory card, and 25b. The wiring 26a and 26b of a predetermined pattern is formed in the inside of Substrates 25a and 25b. The top-face lateral electrode 3 and the inferior-surface-of-tongue lateral electrode 4 of a semiconductor device 1 are electrically connected to said wiring 26a and 26b through conductive jointing materials for corrugated fibreboard, such as solder which is not illustrated. In this example, memory space becomes twice as compared with the case where an SOJ mold semiconductor device is incorporated. Moreover, since the semiconductor device 1 of this operation gestalt has strong structure, its handling nature is good and tends to incorporate it between substrate 25a of a pair, and 25b.
[0026] Although invention made by this invention person above was concretely explained based on the operation gestalt It cannot be overemphasized that it can change variously in the range which this invention is not limited to the above-mentioned operation gestalt, and does not deviate from the summary. If it is in a semiconductor device 1 as shown in drawing 7 In the wiring substrate 2, it considers as the structure of preparing 2nd glass epoxy plate 11b only in the inferior-surface-of-tongue side of the 1st glass epoxy plate 10. Semiconductor device 14a is fixed to component fixed hollow 13a by seat GURI prepared in the center of a top face of said 1st glass epoxy plate 10. It is good also as structure which carried out bonding of the semiconductor device 14b which has the bump electrode 30 in the rear-face side of the 1st glass epoxy plate 10 to wiring 12b with face down structure.
[0027] Moreover, on the top face of the 1st glass epoxy plate 10, a part for the toe of wiring 12a (in this example, it becomes the top-face lateral electrode 3) is connected with the electrode of semiconductor device 14a by wire 15a. In this case, since wire 15a projects rather than the top face of the 1st glass epoxy plate 10, wrap resin 16a projects and (lobe 31) carries out semiconductor device 14a and wire 15a. In this invention, since a semiconductor device 1 serves as structure whose pile is possible, sufficient hollow 32 to enter is formed in 2nd glass epoxy plate 11b stuck on the inferior-surface-of-tongue side of said 1st glass epoxy plate 10 for said lobe 31 for example, of seat GURI.
[0028] Also in this operation gestalt, increase-ization of memory space can be attained by making common the external terminal 3 of the semiconductor devices 14a and 14b which consist of two memory devices, i.e., a top-face lateral electrode, the inferior-surface-of-tongue lateral electrode 4, and the side-face lateral electrode 5. Also in this structure, since the closure object of the two semiconductor devices 14a and 14b is carried out by the strong wiring substrate 2 and Resin 16a and 16b, its handling nature is good.
[0029] Drawing 8 is the sectional view showing the semiconductor device 1 of other operation gestalten of this invention. Two semiconductor devices 14a and 14b in which this operation gestalt is included are not necessarily a memory device. That is, the external drawer terminal of semiconductor device 14a by the side of the top face of the 1st glass epoxy plate 10 serves as the top-face lateral electrode 3 by the side of the top face of the wiring substrate 2, and the external drawer terminal of semiconductor device 14b by the side of the inferior surface of tongue of the 1st glass epoxy plate 10 serves as the inferior-surface-of-tongue lateral electrode 4 by the side of the inferior surface of tongue of the wiring substrate 2. Multichip-ization can be attained with this operation gestalt. Consequently, multi-

functionalization of a semiconductor device 1 can be attained.
[0030]
[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.
[0031] (1) It becomes strong structure and handling nature becomes good from having structure which attached in the hollow on the rear face of front of a wiring substrate object the semiconductor device which constitutes memory, respectively, and covered the semiconductor device by insulating resin.
[0032] (2) Since it has structure which attached in the hollow on the rear face of front of a wiring substrate object the semiconductor device which constitutes memory, respectively, increase of memory space can be aimed at.
[0033] (3) Since it is constituted so that the electrode with which a semiconductor device serves as structure which can be piled up one by one, and a lower semiconductor device and a upside semiconductor device correspond by piling up may be connected, superposition mounting can attain large capacity-ization of memory.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the semiconductor device of 1 operation gestalt of this invention.
[Drawing 2] It is the top view of the semiconductor device in the condition of having cut and lacked a part of this operation gestalt.
[Drawing 3] It is the top view of the wiring substrate in which the wirebonding condition in manufacture of the semiconductor device of this operation gestalt is shown.
[Drawing 4] It is the sectional view showing the condition of having put the semiconductor device of this operation gestalt on multistage.
[Drawing 5] It is the side elevation showing the condition of having mounted two or more semiconductor devices of this operation gestalt in the memory module substrate multistage.
[Drawing 6] It is the sectional view showing the condition of having mounted the semiconductor device of this operation gestalt between the substrates of the pair of a memory card.
[Drawing 7] It is the sectional view showing the semiconductor device of other operation gestalten of this invention.
[Drawing 8] It is the sectional view showing the semiconductor device of other operation gestalten of this invention.
[Description of Notations]
1 [-- Inferior-surface-of-tongue lateral electrode,] -- A semiconductor device, 2 -- A wiring substrate, 3 -- A top-face lateral electrode, 4 5 -- A side-face lateral electrode, 10 -- The 1st glass epoxy plate, 11a, 11b -- The 2nd glass epoxy plate, 12a, 12b -- Internal wiring, 13a, 13b -- A component fixed hollow, 14a, 14b -- Semiconductor device, 15a, 15b [-- A laminating mold

semiconductor device, 22 / -- A memory module substrate, 25a, 25b / -- A substrate 26a, 26b / -- Wiring, 30 / -- An electrode 31 / -- A lobe 32 / -- Hollow.] -- A wire, 16a, 16b -- Resin, 20 -- Solder, 21

[Translation done.]

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	23/12					

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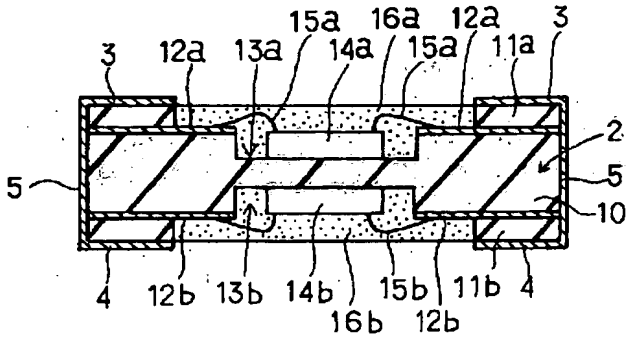
(54)【発明の名称】　半導体装置

(57)【要約】

【課題】　取り扱い性が良好な堅牢な半導体装置の提供。

【解決手段】　表裏面中央に少なくとも一段窪んだ窪みを設けた多層構造の配線基板と、前記配線基板の表裏面の窪みにそれぞれ固定される半導体素子と、前記配線基板の表裏面に設けられかつ所定の内部配線と接続される外部電極と、前記半導体素子の電極と前記内部配線または外部電極とを電気的に接続する接続手段と、前記半導体素子を覆う絶縁性の封止体（レジン）とを有する。前記半導体素子はメモリ素子からなり、前記配線基板の上面側電極および下面側電極は透視的に上下に重なり、相互に重なる電極は同一機能の電極となっている。前記半導体装置は順次重ねることができる構造となり、重ねることによって下部の半導体装置の上面側電極と上部の半導体装置の下面側電極が電気的に接続されるように構成されている。

図１



【特許請求の範囲】

【請求項１】　表裏面中央に少なくとも一段窪んだ窪みを設けた多層構造の配線基板と、前記配線基板の表裏面の窪みにそれぞれ固定される半導体素子と、前記配線基板の表裏面に設けられかつ所定の内部配線と接続される外部電極と、前記半導体素子の電極と前記内部配線または外部電極とを電気的に接続する接続手段と、前記半導体素子を覆う絶縁性の封止体とを有することを特徴とする半導体装置。

【請求項２】　前記半導体素子はメモリ素子からなり、前記配線基板の上面側電極および下面側電極は透視的に上下に重なり、相互に重なる電極は同一機能の電極となっていることを特徴とする請求項１記載の半導体装置。

【請求項３】　前記半導体装置は順次重ねることができる構造となり、重ねることによって下部の半導体装置の上面側電極と上部の半導体装置の下面側電極が電気的に接続されるように構成されていることを特徴とする請求項２記載の半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体装置、特にＬＣＣ(Leadless-chip carrier) 型半導体装置に関する。

【０００２】

【従来の技術】電子機器に組み込まれるメモリの大容量化を図るため、回路基板に多段に半導体装置が組み込まれている。たとえば、日経ＢＰ社発行「ＶＬＳＩパッケージング技術（下）」1993年5月15日発行、P181にはＴＣＰ構造の半導体装置が多段重ねされている例が記載されている。また、特開昭64-1269 号公報には、デュアルインライン形のモジュール基板の表裏面に、リードを付けた半導体チップ（スタティクＲＡＭ）がそれぞれ多段に重ねられている例が示されている。

【０００３】

【発明が解決しようとする課題】メモリの大容量化を図るために、回路基板等のモジュール基板に多段に半導体装置が重ねて実装されている。しかし、ＴＣＰ構造や半導体チップにリードを付けた構造の半導体装置は、堅固でなく取り扱い性が悪い。

【０００４】本発明の目的は、取り扱い性が良好でかつメモリ容量の大型化が図れる半導体装置を提供することにある。

【０００５】本発明の前記ならびにそのほかの目的と新規な特徴は、本明細書の記述および添付図面からあきらかになるであろう。

【０００６】

【課題を解決するための手段】本願において開示される発明のうち代表的なものの概要を簡単に説明すれば、下記のとおりである。

【０００７】（１）表裏面中央に少なくとも一段窪んだ窪みを設けた多層構造の配線基板と、前記配線基板の表裏面の窪みにそれぞれ固定される半導体素子と、前記配線基板の表裏面に設けられかつ所定の内部配線と接続される外部電極と、前記半導体素子の電極と前記内部配線または外部電極とを電気的に接続する接続手段と、前記半導体素子を覆う絶縁性の封止体（レジン）とを有する。前記半導体素子はメモリ素子からなり、前記配線基板の上面側電極および下面側電極は透視的に上下に重なり、相互に重なる電極は同一機能の電極となっている。前記半導体装置は順次重ねることができる構造となり、重ねることによって下部の半導体装置の上面側電極と上部の半導体装置の下面側電極が電気的に接続されるように構成されている。

【０００８】前記（１）の手段によれば、（ａ）複数の配線基板を張り合わせた配線基板体の表裏面の窪みにそれぞれメモリを構成する半導体素子を取り付け、かつ半導体素子を絶縁性のレジンで被った構造となっていることから、メモリ容量が大きい堅固な半導体装置を提供することができる。

【０００９】（ｂ）半導体装置は順次重ねることができる構造となり、重ねることによって下部の半導体装置と上部の半導体装置の対応する電極が接続されるように構成されていることから、重ね合わせ実装により、メモリの大容量化が達成できる。

【００１０】

【発明の実施の形態】以下、図面を参照して本発明の実施の形態を詳細に説明する。なお、発明の実施の形態を説明するための全図において、同一機能を有するものは同一符号を付け、その繰り返しの説明は省略する。

【００１１】図１は本発明の一実施形態の半導体装置を示す断面図、図２は本実施形態の一部を切り欠いた状態の半導体装置の平面図、図３は本実施形態の半導体装置の製造におけるワイヤボンディング状態を示す配線基板の平面図である。

【００１２】本実施形態ではメモリを構成するＬＣＣ型半導体装置に本発明を適用した例について説明する。本実施形態の半導体装置１は、外観的には、図１および図２に示すように、矩形板状の配線基板２と、この配線基板２の表裏面に設けられた上面側電極３および下面側電極４を有している。また、前記上面側電極３および下面側電極４は側面側電極５を介して電気的に接続されている。したがって、本実施形態の半導体装置１においては、上面側電極３と下面側電極４は、透視的に上下で重なり、相互に重なる電極は同一機能の電極となっている。

【００１３】前記配線基板２は、ガラスエポキシ基板からなり、絶縁性の第１ガラスエポキシ板１０と、前記第１ガラスエポキシ板１０の表裏面に張り付けられた枠状の第２ガラスエポキシ板１１ａ，１１ｂとからなっている。したがって、配線基板２の表裏面中央は一段窪んだ構造となる。

【００１４】前記第１ガラスエポキシ板１０の表裏面には、図１乃至図３に示すように、所定パターンの配線（内部配線）１２ａ，１２ｂが設けられている。内部配線１２ａ，１２ｂの第１ガラスエポキシ板１０の縁に延在する外端部分は、透視的に見て前記上面側電極３および下面側電極４と重なるようになっている。そして、内部配線１２ａ，１２ｂの外端部分は前記上面側電極３や下面側電極４に電気的に繋がる側面側電極５に電気的に接続されている。また、内部配線１２ａ，１２ｂは透視的に見て相互に重なるパターンとなっている。

【００１５】また、前記第１ガラスエポキシ板１０の中央には座グリによって半導体素子を固定するための素子固定窪み１３ａ，１３ｂが設けられている。これにより、配線基板２の表裏面中央は二段窪み構造となっている。

【００１６】前記素子固定窪み１３ａ，１３ｂには、それぞれ図示しない接着剤を介してメモリ素子を構成する半導体素子１４ａ，１４ｂが固定されている。前記半導体素子１４ａ，１４ｂの図示しない電極と、内部配線１２ａ，１２ｂの内端部分は、導電性のワイヤ１５ａ，１５ｂで電気的に接続されている。

【００１７】また、前記配線基板２の表裏面の窪んだ部分には、絶縁性のレジン（封止体）１６ａ，１６ｂが埋め込まれ、半導体素子１４ａ，１４ｂやワイヤ１５ａ，１５ｂを封止するようになっている。レジン１６ａ，１６ｂの表面は配線基板２の表裏面の表面と略同一の平面となるような平面となっている。この結果、２つの半導体素子１４ａ，１４ｂは、配線基板２とレジン１６ａ，１６ｂとからなるパッケージによって封止されることになる。

【００１８】本実施形態の半導体装置は薄型，小型な構造となる。たとえば、半導体装置１は、長さ１６．１ｍｍ、幅９．６ｍｍ、高さ１．２～１．５ｍｍ程度となる。

【００１９】本実施形態の半導体装置１は、前記配線基板２の窪んだ表裏面にそれぞれメモリ素子からなる半導体素子１４ａ，１４ｂが固定され、各半導体素子１４ａ，１４ｂの外部引出し端子（上面側電極３，下面側電極４，側面側電極５）が共通となるため、メモリ容量は高いものとなる。すなわち、メモリ容量は単一の半導体素子を内蔵した半導体装置の２倍のメモリ容量を有することになる。

【００２０】本実施形態の半導体装置１は、堅固な配線基板２の窪み内に内蔵され、かつレジン１６ａ，１６ｂで覆われるため、堅固な構造となり、取り扱い性が良好となる。

【００２１】本実施形態の半導体装置１は、配線基板２の第１ガラスエポキシ板１０に座グリ部分を設け、その座グリ部分に半導体素子１４ａ，１４ｂを固定する構造となるため、高さが配線基板２の厚さとなり薄型構造となる。

【００２２】このような本実施形態の半導体装置１は、単品での使用も可能であるが、上面側電極３および下面側電極４が透視的に上下で重なり、相互に重なる電極は同一機能の電極となっていることから、多層に複数重ねて使用することもできる。

【００２３】すなわち、図４は２つの半導体装置１を電極部分で半田２０を介して重ねて接続した積層型半導体装置２１である。この積層型半導体装置２１は、単一の半導体素子を組み込んだ半導体装置に比較してメモリ容量を４倍に増大させることができる。

【００２４】前記積層型半導体装置２１は、たとえば、図５に示すように、ＳＩＭＭ（Single in-line memory module）基板、すなわちメモリモジュール基板２２の表裏面に並んで複数実装される。本実施形態の半導体装置１は、長さ１６．１ｍｍ、幅９．６ｍｍ、高さ１．２～１．５ｍｍ程度となり、通常のＳＯＪ型半導体装置の半分の高さとなっていることから、単一の積層型半導体装置２１をメモリモジュール基板２２に実装した場合、実装体積が同一であってもメモリ容量は４倍にもなる。これにより、Ｓ.ＩＭＭのメモリ容量を飛躍的に増大させることができる。積層型半導体装置２１も堅固な構造となっていることから、取り扱い性が良く、メモリモジュール基板２２への組み込みも容易となる。

【００２５】図６は本実施形態の半導体装置１をメモリカードの一対の基板２５ａ，２５ｂ間に実装した状態を示す断面図である。基板２５ａ，２５ｂの内面には、所定パターンの配線２６ａ，２６ｂが設けられている。半導体装置１の上面側電極３および下面側電極４は図示しない半田等の導電性接合材を介して前記配線２６ａ，２６ｂに電気的に接続されている。この例では、ＳＯＪ型半導体装置を組み込んだ場合に比較してメモリ容量は２倍となる。また、本実施形態の半導体装置１は堅固な構造となっていることから、取り扱い性が良く、一対の基板２５ａ，２５ｂ間に組み込み易い。

【００２６】以上本発明者によってなされた発明を実施形態に基づき具体的に説明したが、本発明は上記実施形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない、たとえば、図７に示すように、半導体装置１にあっては、配線基板２において、第１ガラスエポキシ板１０の下面側にのみ第２ガラスエポキシ板１１ｂを設ける構造とし、前記第１ガラスエポキシ板１０の上面中央に設けた座グリによる素子固定窪み１３ａに半導体素子１４ａを固定し、第１ガラスエポキシ板１０の裏面側にバンプ電極３０を有する半導体素子１４ｂを配線１２ｂにフェイスダウン構造でボンディングした構造としてもよい。

【００２７】また、第１ガラスエポキシ板１０の上面では、半導体素子１４ａの電極と配線１２ａ（この例では上面側電極３となる）の内端部分をワイヤ１５ａで接続

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してある。この場合、ワイヤ１５ａは第１ガラスエポキシ板１０の上面よりも突出することから、半導体素子１４ａやワイヤ１５ａを覆うレジン１６ａは突出（突出部３１）する。本発明では、半導体装置１は積み重ねができる構造となることから、前記第１ガラスエポキシ板１０の下面側に張り付けられる第２ガラスエポキシ板１１ｂには、前記突出部３１が入り込むに充分な窪み３２が、たとえば座グリによって形成されている。

【００２８】本実施形態においても、２つのメモリ素子からなる半導体素子１４ａ，１４ｂの外部端子、すなわち、上面側電極３，下面側電極４，側面側電極５を共通とすることによってメモリ容量の増大化が図れる。この構造においても、２つの半導体素子１４ａ，１４ｂは、堅固な配線基板２とレジン１６ａ，１６ｂによって封止体されていることから、取り扱い性が良い。

【００２９】図８は本発明の他の実施形態の半導体装置１を示す断面図である。この実施形態は、組み込まれる２つの半導体素子１４ａ，１４ｂはメモリ素子とは限らない。すなわち、第１ガラスエポキシ板１０の上面側の半導体素子１４ａの外部引出端子は配線基板２の上面側の上面側電極３となり、第１ガラスエポキシ板１０の下面側の半導体素子１４ｂの外部引出端子は配線基板２の下面側の下面側電極４となる。本実施形態では、マルチチップ化が達成できる。この結果、半導体装置１の多機能化が達成できる。

【００３０】

【発明の効果】本願において開示される発明のうち代表的なものによって得られる効果を簡単に説明すれば、下記のとおりである。

【００３１】（１）配線基板体の表裏面の窪みにそれぞれメモリを構成する半導体素子を取り付け、かつ半導体素子を絶縁性のレジンで被った構造となっていることから、堅固な構造となり、取り扱い性が良好となる。

【００３２】（２）配線基板体の表裏面の窪みにそれぞれメモリを構成する半導体素子を取り付けた構造となっていることから、メモリ容量の増大が図れる。

【００３３】（３）半導体装置は順次重ねることができる構造となり、重ねることによって下部の半導体装置と上部の半導体装置の対応する電極が接続されるように構成されていることから、重ね合わせ実装により、メモリの大容量化が達成できる。

【図面の簡単な説明】

【図１】本発明の一実施形態の半導体装置を示す断面図である。

【図２】本実施形態の一部を切り欠いた状態の半導体装置の平面図である。

【図３】本実施形態の半導体装置の製造におけるワイヤボンディング状態を示す配線基板の平面図である。

【図４】本実施形態の半導体装置を多段に重ねた状態を示す断面図である。

【図５】本実施形態の半導体装置をメモリモジュール基板に多段に複数実装した状態を示す側面図である。

【図６】本実施形態の半導体装置をメモリカードの一対の基板間に実装した状態を示す断面図である。

【図７】本発明の他の実施形態の半導体装置を示す断面図である。

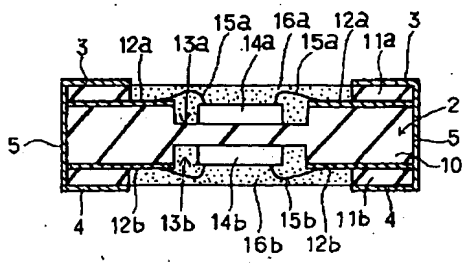
【図８】本発明の他の実施形態の半導体装置を示す断面図である。

【符号の説明】

１…半導体装置、２…配線基板、３…上面側電極、４…下面側電極、５…側面側電極、１０…第１ガラスエポキシ板、１１ａ，１１ｂ…第２ガラスエポキシ板、１２ａ，１２ｂ…内部配線、１３ａ，１３ｂ…素子固定窪み、１４ａ，１４ｂ…半導体素子、１５ａ，１５ｂ…ワイヤ、１６ａ，１６ｂ…レジン、２０…半田、２１…積層型半導体装置、２２…メモリモジュール基板、２５ａ，２５ｂ…基板、２６ａ，２６ｂ…配線、３０…電極、３１…突出部、３２…窪み。

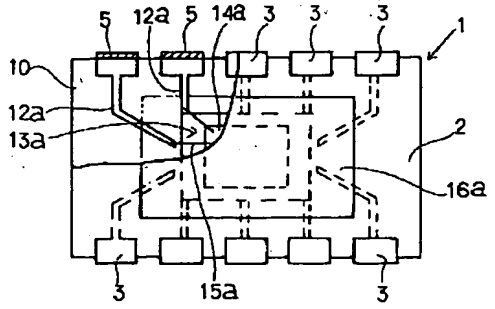
【図１】

図１



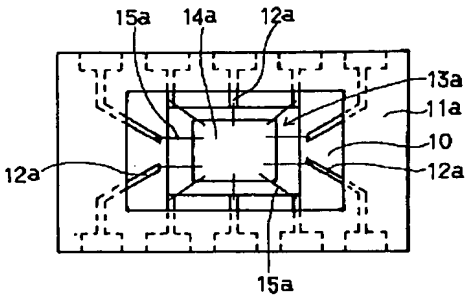
【図２】

図２



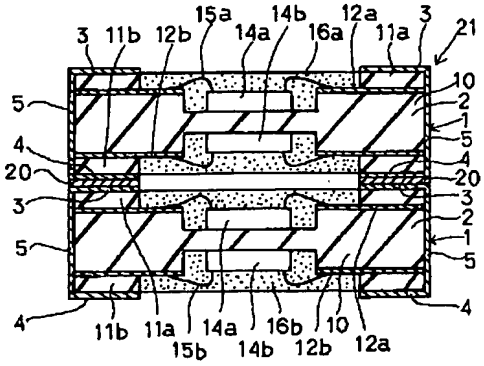
【図３】

図３



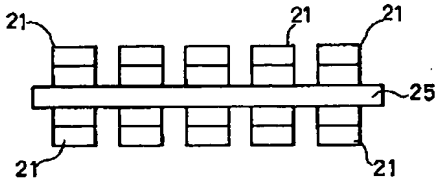
【図４】

図４



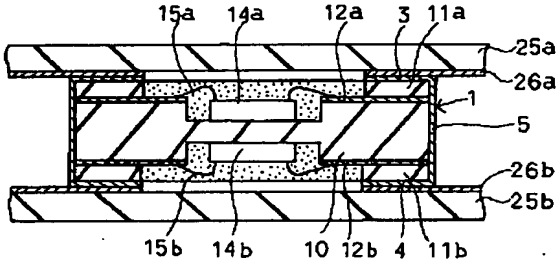
【図５】

図５



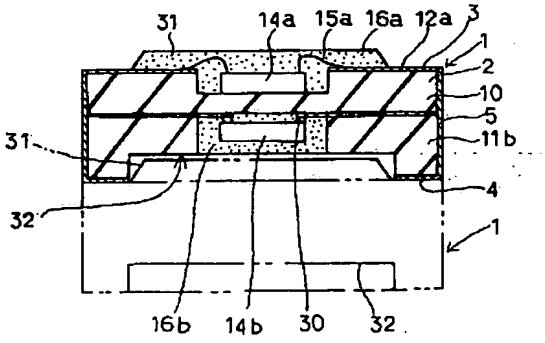
【図６】

図６



【図７】

図７



【図８】

図８